What is claimed is:

1. A semiconductor device, comprising:

a underlayer;

a base oxide film with holes and formed on the underlayer;

a nitride film pattern with a hole pattern formed on the base oxide film and directly above said holes;

an upper oxide film provided on top of said base oxide film to cover the nitride film pattern, the upper oxide film having formed therethrough a wiring groove which exposes part of the nitride film pattern including said hole patterns; and

wiring metal that fills part of the exposed nitride film pattern, said holes, and said wiring grooves;

and wherein said nitride film pattern is formed with such a shape and size that surrounds the outside of said wiring groove and is separate from neighbouring nitride film patterns.

2. A semiconductor device according to claim 1 wherein said nitride film pattern is formed with such a shape and size that surrounds the outside of said wiring groove with a gap from 0.2 to 1.0 μm.

3. A semiconductor device, comprising:

a underlayer;

a base oxide film with holes formed on the underlayer;

a nitride film pattern with hole pattern provided on the base oxide film and formed directly above said holes;

an upper oxide film provided on top of said base oxide film to cover the nitride film pattern, the upper oxide film

having formed therethrough a wiring groove which exposes part of the nitride film pattern including said hole patterns; and

wiring metal that fills part of the exposed nitride film pattern, said holes, and said wiring grooves;

and wherein outer shape of said nitride film pattern is substantially the same as the shape of the opening of said wiring groove, and wherein internal wall surface of said wiring groove is tapered from the opening on the upper surface of said upper oxide film to upper surface of said nitride film pattern.

4. A semiconductor device, comprising:

a underlayer;

a base oxide film formed on the underlayer, the base oxide film having formed therethrough a hole;

an upper oxide film provided on the base oxide film, the upper oxide film having formed therethrough wiring grooves which are connected to said holes; and

wiring metal that fills said holes and said wiring grooves.

5. A semiconductor device according to claim 1, wherein part of the upper surface of said underlayer constitutes the base wiring area, said hole reaches the base wiring area, and a dispersion protection film is formed only on said base wiring area outside the hole.

6. A semiconductor device according to claim 2, wherein part of the upper surface of said underlayer constitutes the base wiring area, said hole reaches the base wiring area, and a dispersion protection film is formed only on said base wiring

area outside the hole.

7. A semiconductor device according to claim 3, wherein part of the upper surface of said underlayer constitutes the base wiring area, said hole reaches the base wiring area, and a dispersion protection film is formed only on said base wiring area outside the hole.

8. A semiconductor device according to claim 4, wherein part of the upper surface of said underlayer constitutes the base wiring area, said hole reaches the base wiring area, and a dispersion protection film is formed only on said base wiring area outside the hole.

9. A semiconductor device manufacturing method comprising the steps of:

forming a base oxide film on a underlayer;

forming a nitride film pattern with hole pattern on the base oxide film;

forming an upper oxide film on said base oxide film so as to cover the nitride film pattern;

forming wiring grooves to expose said nitride film pattern through the upper oxide film and subsequently forming holes to expose part of said underlayer through the base oxide film while using the nitride film patterns as a mask, both by the use of etching processing; and

filling said holes and said wiring grooves with wiring metal;

wherein said nitride film pattern is formed with such a shape and size that the profile of the nitride film pattern

surrounds said wiring grooves.

10. A semiconductor device manufacturing method according to claim 9, wherein profile of said nitride film pattern is formed with such a shape and size that surrounds said wiring groove with a gap from 0.2 and 1.0 μm.

11. A semiconductor device manufacturing method, comprising the steps of:

forming a base oxide film on a underlayer;

forming a groove for nitride film pattern formation within the area of the base oxide film;

filling the groove for nitride film pattern formation with nitride film material and forming a nitride film pattern with a hole pattern;

forming an upper oxide film on said base oxide film that includes the nitride film pattern;

forming wiring grooves to expose part of said nitride film pattern including said hole pattern through the upper oxide film and subsequently forming holes to expose part of said underlayer through said base oxide film within the hole pattern, both by the use of etching processing; and

filling said holes, part of the exposed nitride film pattern, and said wiring grooves with wiring metal.

12. A semiconductor device manufacturing method, comprising the steps of:

forming a base oxide film on a underlayer;

forming a groove on the base oxide film with an opening that is the same shape as a wiring groove to be formed later;

forming a nitride film on the base oxide film including the grooves;

etching the nitride film to form a nitride film pattern having a hole pattern substantially at the center of said groove, with such a shape and size that surrounds the outside of said groove;

forming an upper oxide film on said base oxide film and the nitride film pattern thereon;

forming wiring grooves to expose part of said nitride film pattern including said hole pattern through the upper oxide film and subsequently forming holes to expose part of said underlayer through said base oxide film within the hole pattern, both by the use of etching processing; and

filling said holes, part of exposed nitride film pattern area, and said wiring grooves with wiring metal.

13. A semiconductor device manufacturing method comprising the steps of:

forming a base oxide film on a underlayer;

forming a nitride film pattern with a hole pattern on the base oxide film over an area that surrounds the outside of wiring grooves to be formed later;

forming a side wall formation groove at least on base oxide film exposed from said hole pattern by etching the area of said base oxide film exposed from said nitride film pattern while using the nitride film pattern as a mask;

forming a side wall film within said side wall formation groove and on said nitride film pattern;

forming side walls on side walls of said side wall formation groove by etching the side wall film to exposes the surface of said nitride film pattern;

forming upper oxide film on the side walls, on the base oxide film exposed from the side walls, and on said nitride film pattern;

forming wiring grooves to expose part of said nitride film pattern including said hole pattern through the upper oxide film and subsequently forming holes to expose part of said underlayer through said base oxide film within the hole pattern, both by the use of etching processing; and

filling said holes, exposed side walls, part of the exposed nitride film pattern, and said wiring grooves with wiring metal.

14. A semiconductor device manufacturing method comprising the steps of:

forming a base oxide film on a underlayer;

forming a groove on the base oxide film with an opening that is shaped in the same way as the wiring groove to be formed later;

forming a side wall film on the base oxide film, including the groove;

forming a side wall on the sides of the groove by etching said side wall film to expose the surface of said base oxide film;

forming a nitride film pattern with a hole pattern on the side walls, in the groove exposed from the side walls, and

on the area of said base oxide film around the grooves;

forming an upper oxide film on said base oxide film including the nitride film pattern;

forming wiring grooves to expose part of said nitride film pattern including said hole pattern through the upper oxide film and subsequently forming holes to expose part of said underlayer through said base oxide film within the hole pattern, both by the use of etching processing; and

filling said holes, part of exposed nitride film pattern, and said wiring grooves with wiring metal.

15. A semiconductor device manufacturing method comprising the steps of:

forming a base oxide film on a underlayer;

forming a nitride film pattern with hole pattern on the base oxide film;

forming an upper oxide film on said base oxide film to cover the nitride film pattern;

forming wiring grooves to expose part of said nitride film pattern through the upper oxide film and subsequently forming holes to expose part of said underlayer through said base oxide film within the hole pattern, both by the use of etching processing; and

filling said holes and said wiring grooves with wiring metal;

wherein the profile of said nitride film pattern is formed with substantially the same shape as the opening of said wiring groove; and

wherein dry etching is used for continuous formation of said wiring grooves and holes, and the etching gas contains CH_2F_2 gas.

16. A semiconductor device manufacturing method according to claim 15, further comprising a step of etching off part of the nitride film pattern exposed at least from said wiring grooves under a condition that the etching selection rate on the nitride film to the oxide film is high, before the step of filling said wiring metal, and after the step of continually forming said wiring grooves and holes.

17. A semiconductor device manufacturing method according to claim 16, wherein said removal by etching is implemented using dry etching with a fluorine gas.

18. A semiconductor device manufacturing method according to claim 16 wherein said removal by etching is implemented using wet etching.

19. A semiconductor device manufacturing method according to claim 9 further comprising, before the step of forming said base oxide film, the steps of:

forming a dispersion protection film on top of said underlayer; and

patterning the dispersion prevention film so that it remains only on the base wiring area of said underlayer.